

## **SHM-50**

Miniature, High-Speed, Complete ±0.05% Sample Hold Amplifiers



#### **FEATURES**

- Small 8-pin DIP or SMT package
- 30ns typical acquisition time to ±0.01%, 40ns typical acquisition time to 0.005%
- 15ns typical sample-to-hold settling time to ±0.01%
- 100MHz small signal bandwidth
- –78dB feedthrough attenuation
- ±2 picoseconds aperture uncertainty
- 85mW typical, 135mW maximum power dissipation

#### **GENERAL DESCRIPTION**

Murata Power Solution's SHM-50 is a high-speed, highly accurate sample/hold designed for precision, high-speed analog signal processing applications. The SHM-50 features excellent dynamic specifications including a maximum acquisition time of only 40 nanoseconds for a 2V step to  $\pm 0.01\%$ .

Sample-to-hold settling time, to  $\pm 0.01\%$  accuracy, is 20 nanoseconds maximum with an aperture uncertainty of  $\pm 2$  picoseconds.

The SHM-50 is a complete sample/hold circuit, containing a precision MOS hold capacitor and a MOSFET switching configuration which results in faster switching and better feedthrough attenuation. Additionally, a FET input amplifier design allows faster acquisition and settling times while maintaining a considerably lower droop rate.



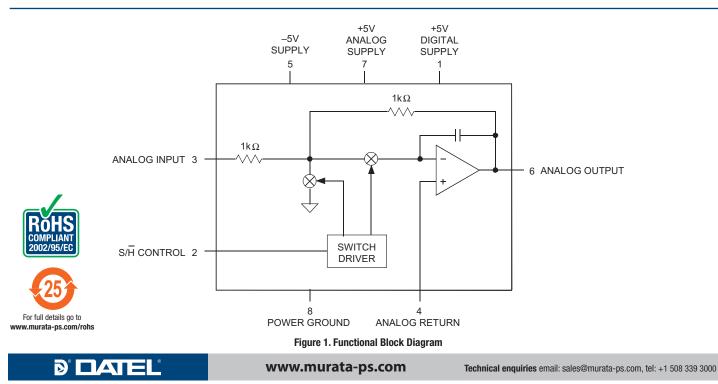
#### **INPUT/OUTPUT CONNECTIONS**

#### Pin Function

- 1 +5v Digital Supply
- 2 S/H Control
- 3 Analog Input
- 4 Analog Return
  - 5 –5v Supply

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- 6 Analog Output
- 7 +5v Analog Supply
  - Power Ground



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# **SHM-50**

#### **Absolute Maximum Ratings**

±5V Supply Voltages	±6.6V
Analog Input	±4V
Digital Input	-0.5V to +5.5V
Output Current	+55 mA
Output Current	±65 mA

#### **Functional Specifications**

Apply over the operating temperature range with  $\pm 5$ Vdc unless otherwise specified.

ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS	
Input/Output Voltage Range	-3.5	_	+3.5	Volts	
Input Impedance	-	1000	—	Ω	
Output Current	-	—	±65	mA	
Output Impedance	-	0.1	_	Ω	
Capacitive Load	100	250	_	pF	
DIGITAL INPUT					
Input Logic Levels					
Logic 1	+2.0	_	+5.0	Volts	
Logic 0	0	_	+0.8	Volts	
Loading					
Logic 1	_	—	+5	μA	
Logic 0	—	—	-5	μA	
TRANSFER CHARACTERISTI	cs				
Gain	_	-1	_	V/V	
Gain Error, +25°C	-	±0.05	±0.25	%	
Linearity Error ①	-	±0.0035	±0.005	%FS	
Sample Mode Offset , +25°C	-	±2	7	mV	
Sample-to-Hold Offset					
(Pedestal), +25°C ②	-	±30	60	mV	
Gain Drift	-	±1	±15	ppm/°C	
Sample Mode Offset Drift ①	-	±3	±15	ppm of	
				FSR/°C	
Sample-to-Hold Off.		_			
(Pedestal) Drift	-	±5	±20	ppm of	
DYNAMIC CHARACTERISTICS	<u> </u>			FSR/°C	
	<b>&gt;</b>				
Acquisition Time					
2V to ±0.005%FS (±100µV)		40	50		
+25°C	_	40	50 TRD	ns	
-55 to +125°C	_	70	TBD	ns	
2V to ±0.01%FS (±200µV) +25°C		20	40		
-55 to +125°C	_	30 40	40 50	ns	
2V to ±0.1%FS (±2mV)	_	40 25	30 30	ns	
Sample-to-Hold Settling Time	_	20	30	ns	
2V to ±0.005%FS (±100µV)		15	25	ns	
2V to ±0.003 % 3 (±100µV) 2V to ±0.01%FS (±200µV)	_	10	20		
Sample-to-Hold Transient		100	20	ns mVp-p	
Aperture Delay Time		2	4	ns	
Aperture Uncertainty (Jitter)		±2	4 ±4	ps	
Output Slew Rate	600	±650	<u>_</u>	V/µs	
Small Signal BW (–3dB)	90	100	_	ν/μs MHz	
Output Droop	30	100		IVII IZ	
+25°C	_	±0.2	±1.0	µV/nS	
0 to +70°C		±0.2 ±0.3	±1.0 ±1.0	μν/n3 μV/nS	
-55 to +125°C		±0.3 ±5.0	±12.0	μν/n3 μV/nS	
Feedthrough Rejection		±3.0 78	±12.0	dB	
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POWER REQUIREMENTS	MIN.	TYP.	MAX.	UNITS
Voltage Range				
+5V Supply	+4.75	+5.0	+5.25	Volts
–5V Supply	-4.75	-5.0	-5.25	Volts
Power Supply Rejection Ratio	_	±0.5	±1	mV/V
Quiescent Current Drain				
+5V Analog Supply	_	+7	+12	mA
–5V Supply	—	-10	-15	mA
Power Consumption	_	85	135	mW
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case				
SHM-50MC	0 to +70°C			
SHM-50MM		–55 to +	-125°C	
Storage Temperature Range		–65 to +	-150°C	
Thermal Impedance				
Өјс		15°C	C/W	
өса		35°C	C/W	
Package Type	8-	pin ceramic	DIP or SM	г

#### Footnotes:

① Full Scale (FS) = 2V. Full Scale Range (FSR) = 4V.

2 Sample-to-hold offset error (pedestal) is constant regardless of input/output level.

#### **Ordering Information**

MODEL	OPERATING TEMP. RANGE	PACKAGE
SHM-50MC	0 to +70°C	DIP
SHM-50MM	–55 to +125°C	DIP
SHM-50GC	0 to +70°C	SMT
SHM-50GM	–55 to +125°C	SMT
	of high-reliability versions of the S a Power Solutions.	HM-50,

#### **TECHNICAL NOTES**

- All ground pins should be tied together and connected to system analog ground as close to the package as possible. It is recommended to use a ground plane under the device and solder ground pins directly to it. Take care to ensure that no ground potentials can exist between ground pins. A single +5V supply can be used for both +5V Digital Supply (pin 1) and +5V Analog Supply (pin 7).
- External 0.1µF to 4.7µF tantalum bypass capacitors are required in critical applications.
- 3. A logic 1 on S/H puts the unit in the sample mode. A logic 0 puts the unit in hold mode.



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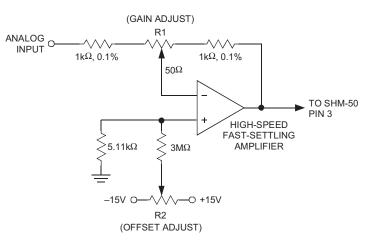
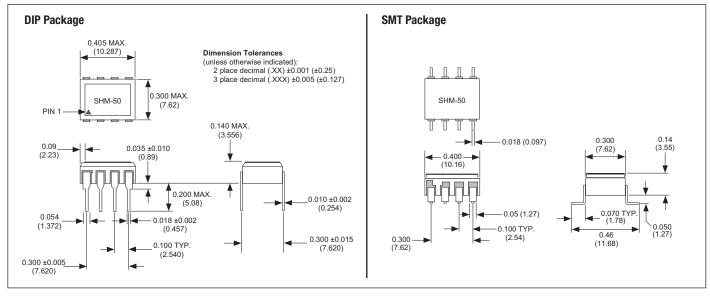


Figure 2. Offset and Gain Adjustments

#### MECHANICAL DIMENSIONS Inches (mm)



ISO 9001 REGISTERED

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